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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,764	11/25/2003	Masashi Yonemaru	829-618	3114

23117 7590 11/18/2005

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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/720,764	Applicant(s) YONEMARU, MASASHI	
	Examiner Thomas L. Dickey	Art Unit 2826	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 27 October 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☐ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1,6,8 and 24*.
   Claim(s) withdrawn from consideration: *2,3,5,7 and 9-23*.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). ____
13. ☒ Other: PTO-892.

Minhloan Tran

Minhloan Tran
Primary Examiner
Art Unit 2826

Continuation of 11. does NOT place the application in condition for allowance because: It is argued that "Taki specifically states that it covers a logic gate cell that includes two inverting logic gates 1 and 2, with an output of the first inverting logic gate 1 connected to one of inputs of the second inverting logic gate 2. The inverting logic gates refer to a NAND gate, a NOR gate, a NOR gate, an AND-OR compound gate and an OR-NAND compound gate as shown in Figs. 1-7 (see col. 9, lines 28-38.). Thus, there is a lack of motivation to combine Taki with Yonemaru, as the D-flip flop of Yonemaru is not an inverting logic gate as disclosed by Taki. Accordingly, it is respectfully requested that the Section 103(a) combination rejection be withdrawn (as to all claims)."
The examiner replies, in the first instance, that it is misleading to state that a "D-flip flop... is not an inverting logic gate." A D-flip flop is a NAND gate latch placed in series with a pulse steering circuit. The Pulse Steering Circuit is to synchronize data capture with external timing, the external timing being either a one-time "enable capture" pulse or more typically a clock pulse. See "The D Flip Flop" (http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/dflipflop.html), Professor Carl R. (Rod) Nave, Department of Physics and Astronomy, Georgia State University (2005). A NAND gate latch, as can be seen in Professor Nave circuit diagram, is a logic gate cell that includes two inverting logic gates 1 and 2, with an output of the first inverting logic gate 1 connected to one of inputs of the second inverting logic gate 2. If this sounds familiar, it is because it is precisely what applicant claims that "Taki specifically states that it covers." In other words Yonemaru's "D flip flop" is simply a slightly more sophisticated version of the NAND gate latch applicant already admits Taki discloses. Furthermore, the reason for the added sophistication would be clear to one having skill in the art. Synchronizing data capture allows that NAND gate latch to capture and hold data until such time as the adjoining circuitry is ready to receive it.
The Examiner replies, secondly, that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In other words Yonemaru's D flip flop need not be bodily incorporated into Taki's device. It is enough that Yonemaru's use of the D flip flop as a data retaining device suggests to one of ordinary skill in the art to modify Taki's second cell so that it functions as at least one of a driver circuit for driving the logic operation circuit or (specifically with respect to claim 24) as a data retaining circuit for retaining data output by the logic operation circuit. .